***Title: High Performance CPU Design and associated HVM/Test Challenges – Shridhar Bendi***

*Speaker will provide basics around building high performance CPU and will cover non-traditional challenges associated with Testing and Productizing SoCs. Unlike traditional ASICs, high end chips have aggressive Power Management states (varying P-States, C-States). And this problem gets compounded further when with on-die Voltage Regulators. There would be mention about growing pains in building SoCs on evolving process node and associated design resilience to work around varying material type over time.*

***Biodata:***

*Shridhar Bendi serves as DFx and Post-Si Debug Lead for Server SoCs designed out of Intel, Bangalore. His most recent contributions include productizing BDX-DE Micro Server and BDX-ML Mainline Servers built on Intel’s 14nm Process node. Prior to joining Intel India design center, he has worked in US with AMD, Texas Instruments, Cyrix and Intel with industry experience of 20+ years of experience. Currently he is Principal Engineer with SDG-India, Bangalore working on the next generation Servers.*

